Amendments to the Specification:

Please replace paragraph [0015] with the following amended paragraph:

[0015] Referring to Fig. 2b, the sacrificial layer is patterned using a photoresist process, and some area on which an MIM capacitor is formed is removed by dry-etch or wet-etch. Then, an upper metal layer 15[[4]] and a dielectric layer 14[[5]] are deposited in sequence. The dielectric layer is formed by chemical vapor deposition or atomic layer deposition using a material such as SiN, SiO_2, Al_2O_3, TaON, TiO_2, Ta_2O_5, ZrO_2, $(Ba,Sr)TiO_3$ (hereinafter referred to as "BST"), $(Pb,Zr)TiO_3$ (hereinafter referred to as "PZT"), or $(Pb,La)(Zr,Ti)O_3$ (hereinafter referred to as "PLZT"). The dielectric layer is a single layer or multi-layer with a thickness of 200~1000Å.